Parallelization of C^3M

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Problem Description

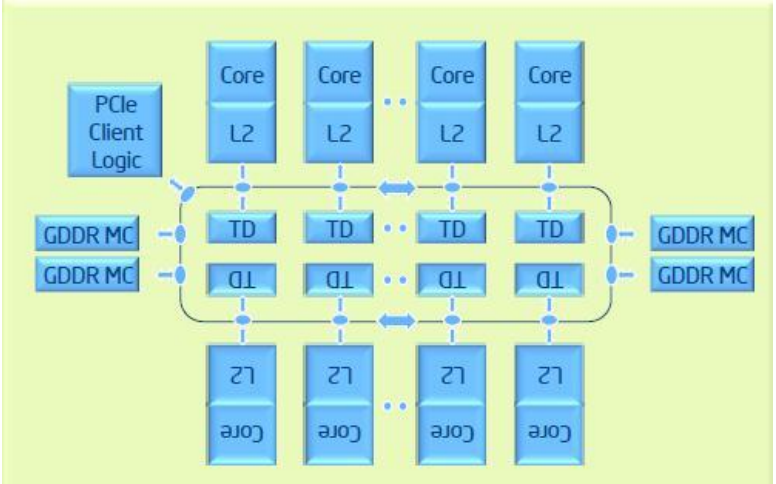
- Cover-Coefficient-based Clustering Methodology [1]
  - Effective
  - Efficient?

Motivation

- Moore's Law [2]
  - Smaller but many core
  - Need parallelism

Motivation

- Intel Xeon Phi [3]
  - Many Integrated Core (MIC) Architecture
  - 60 Cores @ 1.053 GHz with 512 KB L2 cache
  - Ring interconnect
  - 4 hardware threads per core
  - 1 Teraflop/s performance



Methodology

- Implement of C^3M
- Determine parallelizable sections

- Native vs Offload
  - Small cores
    - I/O

- OpenMP[4]
  - Pragamas and Directives

Expected Results

Speed up

Questions and Answers

References

[1] F. Can and E. A. Ozkarahan. Concepts and effectiveness of the cover-coecient-based clustering methodology for text databases. ACM Transactions on Database Systems (TODS), 15(4):483-517, 1990.

[2] Schaller, Robert R. "Moore's law: past, present and future." *Spectrum, IEEE*34.6 (1997): 52-59.

[3] Intel Xeon Phi Coprocessor - the Architecture. https://software.intel.com/en-us/articles/intel-xeon-phi-coprocessor-codename-knights-corner. Accessed: 2015-03-20.

[4] L. Dagum and R. Menon. Openmp: an industry standard api for shared-memory programming. Computational Science & Engineering, IEEE, 5(1):46{55, 1998.