In mathematics and computational geometry, a Delaunay triangulation for a given set P of discrete points in a general position is a triangulation DT(P) such that no point in P is inside the circumcircle of any triangle in DT(P). There are many different algorithms on computing Delaunay triangulation with various optimizations. For the CS564 project, we propose to design and implement an efficient FPGA kernel that will compute Delaunay triangulation.

First a quick survey study on different triangulation algorithms (such as divide-and-conquer and incremental insertion) will be conducted, focusing on the suitability for implementation on FPGA. Then, the most fit algorithm will be further explored for possible FPGA-specific optimizations. The design will be implemented using high-level synthesis and will run on Xilinx UltraScale VCU1525 FPGA. We will evaluate the performance of our design in terms of execution time for different number of points for generated test data, and compare the results to baseline CPU and GPU implementations.

By the time for progress report, it is aimed to deliver the survey and the design, and to have little work on implementation to be remaining if not done. By the time for the final report, it is expected to deliver the final implementation together with experiments.