CS 564 Computational Geometry Project Proposal

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PCB Plane Capacitance Calculator via Polygon Intersection

For the term project of CS 564 Computational Geometry Course, I plan to develop a program that calculates the capacitance between two copper planes in a printed circuit board (PCB). In hardware design, the capacitances on power nets are highly critical as improper capacitance values may lead to faults in the PCB. These capacitances are usually added to the circuit with external components but the copper traces on the PCB itself also have parasitic capacitances. Therefore, the value of these parasitic capacitors may be crucial to the design process.

As the construction of a capacitor requires two parallel conductor plates with a dielectric component in between, the problem can be modeled as a polygon intersection problem. Most PCBs are multi-layered and power lines and return lines are usually on different layers of the PCB. These power and return lines can be modeled as polygons on a plane and the resulting parasitic capacitance is directly correlated to the intersection area. There are example algorithms in the course notes and I will be examining them and doing more research into the topic to create this program.