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EDUCATION

Ph.D. in Computer Science and Engineering, May 2007
The Pennsylvania State University, University Park, PA.

Master of Science in Computer and Information Science and Engineering, August 2002
University of Florida, Gainesville, FL.

Bachelor of Science in Computer Engineering, June 2000
Bogazici University, Istanbul, Turkey

INDUSTRIAL AND ACADEMIC EXPERIENCE

- **Associate Professor, Bilkent University**, Computer Engineering Department, Ankara, Turkey, June 2013 – Present.
- **Visiting Associate Professor, Arizona State University**, Department of Computer Science and Engineering, School of Computing, Informatics and Decision Systems Engineering, Tempe, Arizona, July 2014 – January 2015.
- **Assistant Professor, Bilkent University**, Computer Engineering Department, Ankara, Turkey, January 2008 – May 2013.
- **Senior Researcher, NEC Labs America**, Princeton, New Jersey, January 2011 – September 2011.
- **Visiting Researcher, INRIA**, Paris, France, June 2009 – August 2009, ALCHEMY group (Architectures, Languages and Compilers to Harness the End of Moore Years): Optimization using Polyhedral Model.
- **Senior Software Optimization Engineer, Intel Corporation**, Cellular and Handheld Group - Marvell, April 2006 – January 2008, Chandler, Arizona: Senior Software Optimization Engineer.
- **Research Associate, Processor Architecture Laboratory (LAP), Swiss Federal Institute of Technology of Lausanne (EPFL)**, July 2003 – August 2003, Lausanne, Switzerland: Optimization of a MachSUIF compiler backend for the ARM architecture.
- **Research Assistant/Teaching Assistant, CSE Department**, August 2002 – August 2006, Pennsylvania State University, State College, Pennsylvania.
- **Teaching Assistant, Computer and Information Science and Engineering Department**, August 2000 – May 2002, University of Florida, Gainesville, Florida.

HONORS/AWARDS

- HiPEAC Paper Award, 2016.
- Fulbright Senior Researcher Award, 2014.
- Intel Research Award, 2013.
- Turk Telekom Research Collaboration Award, 2012.
- Associate Professor (Doçent) title from Inter-University Council (UAK) of Turkey, June 2011.
- IBM Faculty Award, 2009.
- European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) Paper Award, 2009.
- EC FP7 Marie Curie Fellowship, 2009.
- Tubitak (Turkish NSF) Incentive Award for European Union FP7 Marie Curie IRG project, 2009.
- The most popular paper from ACM's refereed journals and conference proceedings downloaded, October 2006 (Communications of the ACM, January 2007/Vol. 50, No. 1).
- Best Paper Award from the Twelfth International Conference on Parallel and Distributed Systems (ICPADS'06), Minneapolis, Minnesota, June 2006.
- Nominated for Best Paper Award in DAC-2006 and DAC-2004.

TEACHING EXPERIENCE

- Courses at Bilkent:
 - CS 101 – Algorithms and Programming I (Spring 10)
 - CS 102 – Algorithms and Programming II
 - (Sum 08, 10, 13, 15, 16, 17, Sp 12, 13, 14, 15, 16)
 - CS 223 – Digital Design (Fall 08, 10, 16, Spring 11)
 - CS 224 – Computer Organization (Spring 08, 09, 10, 11, 15, 16, 17, Fall 17)
 - CS 423 – Computer Architecture (Fall 09, Spring 12)
 - CS 426 – Parallel Computing (Fall 15, 16, 17, Spring 12, 13, 14)
 - CS 432 – Machine to Machine Systems (Spring 14, 15)
 - CS 541 – Chip Multiprocessors (Spring 08, 09, Fall 11, 12, 13)
 - CS 590/690 – Research Topics (Fall 08, Spring 10, Fall 10)
 - GE 401-2 Innovative Product Design and Development I-II (Fall 09,11,12, Spring 10,12)
- Past Courses:
 - CSE 203 - Business Programming (Pennsylvania State University, Fall 02)
 - CSE 201C - C++ Programming for Eng. (Pennsylvania State University, Spring 03)
 - COP 3100 - Applications of Discrete Structures (U. Of Florida, Fall 00, Spring 01)
 - COP5725 - Graduate- Database Management Systems (U. Of Florida, Fall 01, Spring 02)
 - COP4720 - Database Management Systems (U. Of Florida, Fall 01, Spring 02)

RESEARCH INTERESTS

Systems/ High Performance Computing:

Accelerator Technologies, Cloud Computing, Heterogeneous Clusters, GPU-based Systems, Efficient Parallelization, Resource Management

Architecture:

Manycore Architectures, Heterogeneous Architectures, Chip Multiprocessors, Reliability, Computer Architecture, Memory Hierarchy

Programming Languages/Compiler:

Compiler Optimizations, Programming Languages, Automatic Parallelization

RESEARCH PROJECTS

- A High Level Design Methodology for Developing Graph Algorithms on Xeon + FPGA Platforms, 2017-2019, Funded by **Intel Corporation**, (with Assist. Prof. Mustafa Ozdal, Bilkent University).
- Safe Computer Design, 2015-101, 2015-2017, Funded by **ASELSAN**.
- Software and Hardware Solutions for Safety Critical Applications, 2106-2018, Funded by **TUBITAK**.
- Using Accelerator Technologies in Graph Parallel Applications, 2013-2015, Funded by **Intel Corporation**.
- CUDA Research Center (CRC), 2013 - 2017, Funded by **NVIDIA**.
- Hardware/Software Mechanisms to Enhance the Effectiveness of Directory Based Cache Coherence in Tiled Chip Multiprocessors (**TUBITAK** - 113E258), 2013-2015, (with Assoc. Prof. Ismail Kadayif, Canakkale Onsekiz Mart University).
- Reliability-Aware Network on Chip (NoC) Architecture Design (**TUBITAK** - 112E360), 2013-2-15, (with Assoc. Prof. Suleyman Tosun, Ankara University).
- Utilizing Accelerator Technologies in the Cloud, Funded by **TÜRK TELEKOM**, 2012-2013.
- Developing Techniques for Automatic Parallelization, Funded by European Network of Excellence on High Performance and Embedded Architecture and Compilation (**HiPEAC**), 2010-2011, (with Prof. Michael O'Boyle, University of Edinburgh)
- Heterogeneous Chip Multiprocessor Design (HTCMP), Funded by European Commission (EC) **FP7-PEOPLE MARIE CURIE ACTIONS**, 2009 – 2013.

- Energy Efficient Application Mapping onto Network-on-Chips with Different Topologies, Funded by The Scientific & Technological Council of Turkey (**TUBITAK** – 108E233), 2009 – 2012, (with Asst. Prof. Suleyman Tosun, Ankara University).
- Utilizing Heterogeneous CMPs through Efficient Parallelization, Funded by **IBM**, 2009-2010.
- Parallelizing for IBM Cell, Funded by EC **FP7** HPC-Europa2, 2009-2010.

PROFESSIONAL ACTIVITIES

- HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation) member.
- GSRC (Gigascale Systems Research Center) member.
- IEEE and ACM member.
- Program/General Chair
 - MSE 2017 – General Chair, Microsystems Education, Banff, Canada, May 2017.
 - ICS 2016 – General Chair, 30th International Conference on Supercomputing, Istanbul, Turkey, June 2016.
 - ASPLOS 2015 – General Chair, 20th International Conference on Architectural Support for Programming Languages and Operating Systems, Istanbul, Turkey, March 2015.
 - MSE 2015 – Program Chair, Microsystems Education, Pittsburgh, Pennsylvania, May 2015.
 - MEDIAN 2014 – Program Co-Chair, Manufacturable and Dependable Multicore Architectures at Nanoscale, Dresden, Germany, March, 2014.
 - MSE 2013 - Registration Chair, Microsystems Education, Austin, Texas
- Program Committee Member
 - DSD 2016 - The 19th Euromicro Conference on Digital Systems Design, Limassol, Cyprus, August 31-September 2, 2016.
 - ASAP 2016 – The 27th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors Jul 6th-8th 2016, London, England.
 - MICRO 2015 ERC - The 48th Annual IEEE/ACM International Symposium on Microarchitecture, December 5-9, 2015, Waikiki, Hawaii.
 - IPDPS 2015 - The 29th IEEE International Parallel & Distributed Processing Symposium will be held at the Hyderabad International Convention Center in Hyderabad, India, during May 25-29, 2015.
 - HiPC 2015 - The 22nd annual IEEE International Conference on High Performance Computing, Data, and Analytics, Bengaluru, India, December 16 - 19, 2015.
 - DSD 2015 – The 18th Euromicro Conference on Digital Systems Design, Funchal, Madeira, Portugal, August 26-28, 2015.
 - PPAM 2015 – 11th International Conference On Parallel Processing And Applied Mathematics, September 6-9, 2015, Krakow, Poland.
 - ASAP 2015 – The 26th IEEE International Conference on Application-specific Systems, Architectures and Processors, July 27-29, 2015, Toronto, Canada.
 - APPT 2015 – International Symposium on Advanced Parallel Processing Technology, August 20-21, 2015, Jinan, Shandong, China.
 - MICRO 2014 – The 47th Annual IEEE/ACM International Symposium on Microarchitecture, December 13-17, 2014, Cambridge, UK.
 - IDT 2014 - 9th International Symposium on Design and Test, December 2014
 - COSMIC 2014 – Code Optimisation for Multi and many Cores" (COSMIC) Workshop
 - DSD 2014 - 17th Euromicro Conference on Digital System Design, August 27-29, 2014, Verona, Italy.
 - VLSI Design 2014 - 27th International Conference on VLSI Design, January, 2014, Mumbai, India.
 - IDT 2013 - 8th International Symposium on Design and Test, December 2013, Marrakesh, Morocco.

- DSD 2013 - 16th Euromicro Conference on Digital System Design, September, 2013, Santander, Cantabria, Spain.
 - RAPIDO 2013 - 5th Workshop on: Rapid Simulation and Performance Evaluation: Methods and Tools, 21 Jan 2013, Berlin, Germany
 - DFR 2013 - Workshop on Design for Reliability 2013, January, Berlin, Germany
 - PPAM 2013 - 10th International Conference on Parallel Processing and Applied Mathematics, Warsaw, Poland.
 - IPDPS 2012-IEEE International Parallel & Distributed Proc. Symp.
 - DSD 2012 - 15th Euromicro Conference on Digital System Design, September 5-8, 2012, Cesme, Izmir, Turkey
 - RAPIDO 2012 - 4th Workshop on: Rapid Simulation and Performance Evaluation: Methods and Tools Saturday 22 Jan 2012, Paris, France
 - DFR 2012 - Workshop on Design for Reliability 2012, January 23-25, 2012 Paris, France
 - MSE 2011 - Registration Chair, Microsystems Education, San Diego, CA
 - IPDPS 2011-IEEE International Parallel & Distributed Proc. Symp., Anchorage, AL
 - ICC 2010 - Advisory Committee Member, International Conference on Computing 2010, New Delhi, India
 - Cost HPCCE 2010: High-Performance Computing on Complex Environments, WG3: Algorithms and tools for mapping and executing applications onto distributed and heterogeneous systems, Heraklion, Crete, Greece, September, 2010 .
 - YKGS'2010 - II. Ulusal Yazılım Kalitesi ve Yazılım Geliştirme Araçları Semp., Istanbul
 - UYMK'2010 - III. Ulusal Yazılım Mimarisi Konferansı, Ankara, Türkiye
 - DSD 2010 - 13th EUROMICRO CONFERENCE ON DIGITAL SYSTEM DESIGN
 - NSS 2010 - 4th International Conference on Network and System Security
 - DSD 2009 - 12th EUROMICRO CONFERENCE ON DIGITAL SYSTEM DESIGN
 - NSS 2009 - 3rd International Conference on Network and System Security
 - ISCIS 2009 - 24th International Symposium on Computer and Information Sciences
 - TTSDP 2009 - Tools and Techniques in Software Development Processes for HPC
 - SMM 2009 - Software Metrics and Measurement
 - SEPA 2009 - Software Engineering Processes and Applications
- Refereeing for Scholarly and Professional Journals
 - IEEE Transactions on Computers
 - IEEE Transactions on Parallel and Distributed Systems
 - IEEE Transactions on Computer Aided Design
 - IEEE Signal Processing Magazine
 - IEEE Transactions on Very Large Scale Integration (VLSI) Systems
 - IEEE Transactions on Education
 - ACM Transactions on Design Automation of Electronic Systems
 - ACM Transactions on Embedded Computing Systems
 - ACM Transactions on Architecture and Code Optimization
 - Elsevier Computer Communications
 - Wiley Concurrency and Computation: Practice and Experience
 - Journal of Computer Science and Technology
 - Journal of Systems and Software
 - Simulation Modelling Practice and Theory
 - Advances in Engineering Software
- Reviewer for several conferences: PACT, EMSOFT, ICCD, CASES, DATE, ISLPED, ISPASS, ISCAS, TVLSI, TODAES, TCAD, Computer Architecture Letters, HiPC, etc.

GRADUATE STUDENT SUPERVISION

- Current
 - Hamzeh Ahangari, PhD
 - Naveed Ul Mustafa, PhD
 - Funda Atik, MS
 - Erdem Derebasoglu, MS
 - Hakan Tasan, MS
 - Kaan Akyol, MS
 - Ebubekir Karabuga, MS
 - Kaan Copur, MS (co-advised with U. Gudukbay)
 -
- Completed
 - Serif Yesil, MS (2016)
 - Azita Nouri, MS (co-advised with C. Alkan) (2016)
 - Mohammad Reza Soltaniyeh, MS (2015)
 - Tuncer Turhan, MS (2014)
 - Habibe Guldaml Ozsema, MS (co-advised with B. Gedik) (2014)
 - Ismail Akturk, MS (2013)
 - Omer Erdil Albayrak, MS (2013)
 - Dilek Demirbas, MS (2011)
 - Atilla Genç, MS (2009)
 - Kadir Akbudak, MS (2009)
 - Can Şardan, MS (2009)

UNDERGRADUATE STUDENT SUPERVISION

- Serif Yesil, 2012
- Engin Kayraklioglu, 2012
- Mustafa Zengin, 2011
- Kamil Akhuseyinoglu, 2010

PUBLICATIONS

Books:

Memory Hierarchy Design For Chip Multiprocessors: A Compiler Directed Approach (Paperback) by Ozcan Ozturk, VDM Verlag Dr. Müller, December, 2008.

Book Chapters:

1. Workload Clustering for Increasing Energy Savings in MPSoCs, by O. Ozturk, M. Kandemir, and S. H. K. Narayanan, Energy Efficient Distributed Computing Systems, John Wiley & Sons Inc., Editor: Albert Zomaya, ISBN: 978-0-470-90875-4, pages 549--565.
2. Improving Multicore System Performance Through Data Compression, by O. Ozturk and M. Kandemir, Programming Multi-core and Many-core Computing Systems, Book Editors Sabri Pllana and Fatos Xhafa, John Wiley & Sons Inc., In Press.
3. Enabling Network Security in HPC Systems Using Heterogeneous CMPs, by O. Ozturk and S. Tosun, High-Performance Computing on Complex Environments, John Wiley & Sons Inc., Editor: Emmanuel Jeannot and Julius Zilinskas, ISBN: 978-1-118-71205-4, pages 383--401.

Patents:

1. Nishkam Ravi, Tao Bao, Ozcan Ozturk, and Srimat Chakradhar. "A COMPILER FOR X86-BASED MANY-CORE COPROCESSORS", Disclosure 11032a (449-241).
2. Nishkam Ravi, Tao Bao, Ozcan Ozturk, and Srimat Chakradhar. "AN OPTIMIZING COMPILER FOR IMPROVING APPLICATION PERFORMANCE ON MANY-CORE COPROCESSORS", Disclosure 11032b (449-242).

Journals:

1. Classifying Data Blocks at Subpage Granularity with an On-Chip Page Table to Improve Coherence in Tiled CMPs, by M. Soltaniyeh, I. Kadayif, and O. Ozturk, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Accepted. [SCI]
2. A Template Based Design Methodology for Graph-Parallel Hardware Accelerators, by A. Ayupov, S. Yesil, M. M. Ozdal, T. Kim, S. Burns, O. Ozturk, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), DOI: 10.1109/TCAD.2017.2706562. [SCI]
3. Graph Analytics Accelerators for Cognitive Systems, by Muhammet Mustafa Ozdal, Serif Yesil, Taemin Kim, Andrey Ayupov, John Greth, Steven Burns, and Ozcan Ozturk, IEEE MICRO, Volume: 37, Issue: 1, Pages: 42 - 51, DOI: 10.1109/MM.2017.7, 2017. [SCI]
4. Optimization-Based Power and Thermal Management for Dark Silicon Aware 3D Chip Multiprocessors Using Heterogeneous Cache Hierarchy, by A. Asad, M. Fathy, M. R. J. Motlagh, O. Ozturk, Microprocessors and Microsystems (MICPRO), Accepted. [SCI-E]
5. Cache Hierarchy-Aware Query Mapping On Emerging Multicore Architectures, by Ozcan Ozturk, Umut Orhan, Wei Ding, Praveen Yedlapalli, Mahmut Kandemir, IEEE Transactions on Computers (TC), Accepted. [SCI]
6. Pipelined Fission for Stream Programs with Dynamic Selectivity and Partitioned State, Bugra Gedik, Habibe G Özsema, Ozcan Ozturk, Journal of Parallel and Distributed Computing, 96: 106-120, 2016. [SCI]
7. Fault-Tolerant Topology Generation Method for Application-Specific Network-on-Chips, by Tosun, S.; Ajabshir, V.; Mercanoglu, O.; Ozturk, O. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, doi: 10.1109/TCAD.2015.2413848. [SCI]
8. Application mapping algorithms for mesh-based network-on-chip architectures, by Suleyman Tosun, Ozcan Ozturk, Erencaan Ozkan and Meltem Ozen, The Journal of Supercomputing, Volume 71, Issue 3, Pages 995-1017, 2015. [SCI]
9. Energy Reduction in 3D NoCs Through Communication Optimization, O. Ozturk, I. Akturk, I. Kadayif, and S. Tosun, Computing, Vol 97, Issue 6, Pages 593-609, 2015 [SCI]
10. Voltage Island Based Heterogeneous NoC Design Through Constraint Programming, by Ayhan Demiriz, Nader Bagherzadeh, Ozcan Ozturk. Computers and Electrical Engineering, Computers & Electrical Engineering, Volume 40, Issue 8, Pages 307-316, 2014. [SCI-E]
11. Application-Specific Heterogeneous Network-on-Chip Design, by Dilek Demirbas; Ismail Akturk; Ozcan Ozturk; Ugur Gudukbay. The Computer Journal, Volume 57, Issue 8, pages 1117-1132, August 2014. [SCI-E]
12. Improving Application Behavior on Heterogeneous Manycore Systems Through Kernel Mapping, by O. Erdil Albayrak, Ismail Akturk, and Ozcan Ozturk, Parallel Computing, Volume 39, Issue 12, December 2013, Pages 867-878. [SCI]
13. A Decoupled Local-Memory Allocator, by B. Diouf, C. Hantas, A. Cohen, O. Ozturk, and J. Palsberg, ACM Transactions on Architecture and Code Optimization (TACO), Vol. 9, No. 4, Article 34, Publication date: January 2013. [SCI-E]
14. Compiler-Directed Energy Reduction Using Dynamic Voltage Scaling and Voltage Islands for Embedded Systems, by O. Ozturk, M. Kandemir, and G. Chen, IEEE Transactions on Computers (TC), Vol. 62, No. 2, pages 268-278, February 2013. [SCI]
15. Hardware/Software Approaches for Reducing the Process Variation Impact on Instruction Fetches, by I. Kadayif, M. Turkcan, S. Kiziltepe, and O. Ozturk, ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 18, Number 4, Pages 54:1-54:23, October 2013. [SCI-E]
16. Reliability-Aware Heterogeneous 3D Chip Multiprocessor Design, by Ismail Akturk and Ozcan Ozturk. Journal of Electronic Testing Theory and Applications, Volume 29, Issue 2, pages 177-184, April 2013. [SCI-E]
17. Reducing Memory Space Consumption Through Dataflow Analysis, by O. Ozturk, Computer Languages, Systems & Structures, Volume 37, Issue 4, October 2011, pages 168-177. [SCI-E]
18. Multicore Education Through Simulation, by O. Ozturk, IEEE Transactions on Education (TE), Volume 54, Issue 2, pages 203-209, May 2011. [SCI]
19. Data Locality and Parallelism Optimization Using A Constraint-Based Approach, by O. Ozturk, Journal of Parallel and Distributed Computing (JPDC), volume 71, issue 2, pages 280-287, 2011. [SCI]
20. Heterogeneous NoC Design Through Evolutionary Computing, by Ozcan Ozturk and Dilek Demirbas, International Journal of Electronics, Francis & Taylor, Volume 97, No. 10, pages 1139-1161, 2010. [SCI]
21. On-Chip Memory Space Partitioning for Chip Multiprocessors using Polyhedral Algebra, by O. Ozturk, M. Kandemir, M. J. Irwin. IET Computers & Digital Techniques, Volume 4, Issue 6, pages 484-498, 2010. [SCI-E]
22. Improving Chip Multiprocessor Reliability Through Code Replication, by Ozcan Ozturk. Computers & Electrical Engineering, Elsevier, Issue 36, pages 480-490, 2010. [SCI-E]
23. Compiler Directed Communication Reliability Enhancement for Chip Multiprocessors, by O. Ozturk, M. Kandemir, S. Narayanan, and M. J. Irwin. ACM SIGPLAN Notices, Vol. 45, No. 4, pp. 85-94, 2010. [SCI-E]
24. Using Data Compression for Increasing Memory System Utilization, by Ozcan Ozturk, Mahmut Kandemir, Mary J. Irwin. IEEE Transactions on Computer Aided Design, Volume 28, Number 6, pages 901-914, June 2009. [SCI]
25. Shared scratch pad memory space management across applications, by O. Ozturk, M. Kandemir, S. W. Son, and I. Kolcu. International Journal of Embedded Systems, Vol. 4, No.1 pp. 54 - 65, 2009.
26. ILP Based Energy Minimization Techniques for Banked Memories, by O. Ozturk and M. Kandemir. ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13, Issue 3, July 2008. [SCI-E]
27. Access Pattern-Based Code Compression For Memory-Constrained Systems, by O. Ozturk, M. Kandemir, and G.

Chen. ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13, Issue 4, September 2008. [SCI-E]

28. Compiler-Directed Energy Optimization for Parallel Disk Based Systems, by S. W. Son, G. Chen, O. Ozturk, M. Kandemir, and A. Choudhary, IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 18, Number 9, pp. 1241-1257, September, 2007. [SCI]
29. Optimizing Array-Intensive Applications for On-Chip Multiprocessors, by I.Kadayif, M.Kandemir, G.Chen, O.Ozturk, M.Karakoy, and U.Sezer. IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 16, Number 5, May 2005. [SCI]
30. An ILP formulation for task scheduling on heterogeneous chip multiprocessors, by S. Tosun, N. Mansouri, and M. Kandemir. Lecture Notes in Computer Science (LNCS) 4263 Springer 2006, ISBN 3-540-47242-8.
31. An ILP-Based Approach to Locality Optimization, by G. Chen, O. Ozturk, and M. Kandemir. Lecture Notes in Computer Science (LNCS) 3602 Springer 2004, Languages and Compilers for High Performance Computing, pages 149-163.
32. Using data compression to increase energy savings in multi-bank memories, by M.Kandemir, O.Ozturk, M.J.Irwin, and I.Kolcu. Lecture Notes in Computer Science (LNCS) 3149 Springer 2004, ISBN 3-540-22924-8, pages 310-317.

Conferences:

1. Reconfigurable Hardened Latch and Flip-Flop for FPGAs, by Hamzeh Ahangari, Ihsen Alouani, Ozcan Ozturk, Smail Niar. IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2017), Bochum, Germany, July 3-5, 2017.
2. Energy Efficient Architecture for Graph Analytics Accelerators, by M. M. Ozdal, S. Yesil, T. Kim, A. Ayupov, J. Greth, S. Burns, O. Ozturk. In Proc. of ACM/IEEE Int'l Symposium on Computer Architecture (ISCA), June 2016.
3. Boosting Performance of Directory-based Cache Coherence Protocols with Coherence Bypass at Subpage Granularity and A Novel On-chip Page Table, by Mohammadreza Soltaniyeh, Ismail Kadayif, and Ozcan Ozturk. In Proceedings of ACM International Conference on Computing Frontiers 2016, May 16 - 18, 2016, Como, Italy.
4. Neighborhood Solidarity SRAM For Reliability Enhancement of SRAM Memories, by Ihsen Alouani, Hamzeh Ahangari, Ozcan Ozturk, Smail Niar. The 17th Euromicro Conference on Digital Systems Design, Limassol, Cyprus, August 31-September 2, 2016.
5. Register file reliability enhancement through adjacent narrow-width exploitation, by Hamzeh Ahangari, Ihsen Alouani, Ozcan Ozturk, Smail Niar and Atika Rivenq. In Proceedings of the 2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2016, Istanbul, Turkey, April 12-14.
6. FPGA implementation of a fault-tolerant application-specific NoC design, by Serif Yesil, Suleyman Tosun, and Ozcan Ozturk. In Proceedings of the 2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2016, Istanbul, Turkey, April 12-14.
7. Adaptive routing framework for network on chip architectures, Naveed Ul Mustafa, Ozcan Ozturk, Smail Niar. In Proceedings of The 8th Workshop on Rapid Simulation and Performance Evaluation Methods and Tools, 18 Jan 2016, Prague, Czech Republic.
8. Implications of Non-Volatile Memory as Primary Storage for Database Management Systems, by Naveed Ul Mustafa, Adria Armejach, Ozcan Ozturk, Adrian Cristal and Osman Unsal. Proceedings of the 16th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XVI), Samos, Greece, July 18-21, 2016.
9. Proceedings of the 2016 International Conference on Supercomputing, ICS 2016, by Ozcan Ozturk, Kemal Ebcioğlu, Mahmut T. Kandemir, and Onur Mutlu. Istanbul, Turkey, June 1-3, 2016.
10. Architectural Requirements for Energy Efficient Execution of Graph Analytics Applications, by Muhammet Mustafa Ozdal, Serif Yesil, Taemin Kim, Andrey Ayupov, Steven M. Burns, Ozcan Ozturk, ICCAD 2015: 676-681.
11. Hardware Accelerator Design for Data Centers, by Serif Yesil, Muhammet Mustafa Ozdal, Taemin Kim, Andrey Ayupov, Steven M. Burns, Ozcan Ozturk, ICCAD 2015: 770-775.
12. Hybrid Stacked Memory Architecture for Energy Efficient Embedded Chip-Multiprocessors Based on Compiler Directed Approach, by S. Onori, A. Asad, O. Ozturk, and M. Fathy. In Proc. of The 6th International Green And Sustainable Computing Conference (IGSC'15), Las Vegas, Nevada, USA, December, 2015.
13. Exploiting Heterogeneity in Cache Hierarchy in Dark- Silicon 3D Chip Multi-Processors, Arghavan Asad, Ozcan Ozturk, Mahmood Fathy and Mohammad Reza Jahed-Motlagh. In Proc. of The 18th Euromicro Conference on Digital Systems Design, Funchal, Madeira, Portugal in August 26-28, 2015.
14. JSRAM: A Circuit-level Technique for Trading-off Robustness and Capacity in Cache Memories, by Hamzeh Ahangari, Gulay Yalcin, Ozcan Ozturk, Osman Unsal, and Adrian Cristal. In Proc. of IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2015, Montpellier, France, July 8-10, 2015.
15. Proceedings of the Twentieth International Conference on Architectural Support for Programming Languages and Operating Systems, by Ozcan Ozturk, Kemal Ebcioğlu, and Sandhya Dwarkadas, ASPLOS '15, Istanbul, Turkey, March 14-18, 2015. ACM 2015, ISBN 978-1-4503-2835-7.
16. Fault Tolerant Irregular Topology Design Method for Network-on-Chips, by Suleyman Tosun, Vahid Babaei Ajabshir, Ozge Mercanoglu, and Ozcan Ozturk. In Proc. of The 17th Euromicro Conference on Digital Systems Design, Verona, Italy, August 27-29, 2014.
17. AutopaR: An Automatic Parallelization Tool for Recursive Calls, by Mert Emin Kalender, Cem Mergenci, and Ozcan Ozturk. In Proc. of The 43rd International Conference on Parallel Processing (ICPP-2014), The Fifth International Workshop on Parallel Software Tools and Tool Infrastructures (PSTI 2014), Minneapolis, MN, September, 2014.

18. Adaptive Compute-phase Prediction and Thread Prioritization to Mitigate Memory Access Latency, by Ismail Akturk and Ozcan Ozturk. In Proc. of International Workshop on Manycore Embedded Systems, June 2014, Minneapolis, MN.
19. Staggered Latch Bus: A Reliable Offset Switched Architecture for Long On-Chip Interconnect, by Melvin Eze, Ozcan Ozturk, and Vijaykrishnan Narayanan. 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Istanbul, Turkey, October 2013.
20. A Decoupled Local-Memory Allocator, Boubacar Diouf, Can Hantas, Albert Cohen, Jens Palsberg, and Ozcan Ozturk. 8th International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC'13), Berlin, Germany, January 2013.
21. ILP-Based Communication Reduction for Heterogeneous 3D Network-on-Chips, Ismail Akturk and Ozcan Ozturk. In Proc. of 21st Euromicro International Conference on Parallel, Distributed and Networked-Based Processing (PDP'13), Belfast, Northern Ireland, February 2013.
22. Effective Kernel Mapping for OpenCL Applications in Heterogeneous Platforms, by O. E. Albayrak, I. Akturk, and O. Ozturk. In Proc. of The Fifth International Workshop on Parallel Programming Models and Systems Software for High-End Computing (P2S2), September 2012, Pittsburgh, PA, USA.
23. Reliability-Aware 3D Chip Multiprocessor Design, by I. Akturk and O. Ozturk. In Proc. of Median 2012 Workshop, May 2012, Annecy, France.
24. Code Scheduling for Optimizing Parallelism and Data Locality, by T. Yemliha, M. Kandemir, O. Ozturk, E. Kultursay, and S.P.Muralidhara. In Proc. of Euro-Par September 2010, Ischia, Italy.
25. Mapping Applications on Autonomic Network-On-Chip Architectures (poster), by C. Hantas and O. Ozturk. ACM SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems (LCTES) 2010 WiP-PS, Stockholm, Sweden, April 2010.
26. Integer Linear Programming Based Mission Planning for UAVs, by O. Ozturk and C. Hantas. In Proc. of International Unmanned Vehicles Workshop-UVW2010, Istanbul, Turkey, June 2010.
27. Optimizing Shared Cache Behavior of Chip Multiprocessors, by M. Kandemir, S.P.Muralidhara, S. Narayanan, Y. Zhang, and O. Ozturk. In Proc. of The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'09), New York City, NY, December 2009.
28. Slicing Based Code Parallelization for Minimizing Interprocessor Communication, by M. Kandemir, Y. Zhang, S. P. Muralidhara, O. Ozturk and S. Narayanan. In Proc. of CASES'09, Grenoble, France, October 2009.
29. Optimizing Scratch-Pad Memory Allocation and Assignment Through a Decoupled Approach, Boubacar Diouf, Ozcan Ozturk, and Albert Cohen. In Proc. of the 22nd International Workshop on Languages and Compilers for Parallel Computing (LCPC'09), October 2009, Newark, Delaware.
30. An ILP Formulation for Application Mapping onto Network-on-Chips, by S. Tosun, O. Ozturk, M. Ozen. In Proc. of The 3rd IEEE International Conference on Application of Information and Communication Technologies (AICT'09), Baku, Azerbaijan, October 2009.
31. Multicore Education Through Simulation, Ozcan Ozturk. In Proc. Of Microelectronic Systems Education (MSE'09), July 2009, San Francisco, CA.
32. Dynamic Thread and Data Mapping for NoC Based CMPs, Mahmut Kandemir, Ozcan Ozturk, and S.P.Muralidhara. In Proc. of 46th Design Automation Conference (DAC'09), July 2009, San Francisco, CA.
33. Heterogeneous Chip Multiprocessor Design, Ozcan Ozturk. Designing for embedded parallel computing platforms: architectures, tools, and applications Workshop, Design, Automation and Test in Europe (DATE'09).
34. Using Dynamic Compilation for Continuing Execution Under Reduced Memory Availability, Ozcan Ozturk, Mahmut Kandemir. In Proc. of Design, Automation and Test in Europe (DATE'09), Nice, France, April 2009.
35. Adaptive Prefetching for Shared Cache Based Chip Multiprocessors, Mahmut Kandemir, Yuanrui Zhang, Ozcan Ozturk. In Proc. of Design, Automation and Test in Europe (DATE'09), Nice, France, April 2009.
36. Process Variation Aware Thread Mapping For Chip Multiprocessors by S Hong, S H K Narayanan, and M Kandemir, O Ozturk. In Proc. of Design, Automation and Test in Europe (DATE'09), Nice, France, April 2009.
37. SPM Management Using Markov Chain Based Data Access Prediction, by T. Yemliha, S. Srikantaiah, M. Kandemir, and O. Ozturk. In Proc. International Conference on Computer Aided Design (ICCAD'08), San Jose, CA, November 2008.
38. Prefetch Throttling and Data Pinning for Improving Performance of Shared Caches by O. Ozturk, S. W. Son, M. Kandemir, and M. Karakoy. To appear in Proc. of the ACM/IEEE Conference on High Performance Networking and Computing (SC'08), Austin, TX, Nov 2008.
39. Profiler and Compiler Assisted Adaptive I/O Prefetching for Shared Storage Caches, by S. W. Son, S. P. Muralidhara, O. Ozturk, M. Kandemir, I. Kolcu, and M. Karakoy. In Proc. International Conference on Parallel Architecture and Compilation Techniques PACT-2008 Toronto, Canada October 25-29, 2008.
40. Software-Directed Combined CPU/Link Voltage Scaling for NoC-Based CMPs, by O. Ozturk and M. Kandemir. In Proc. the ACM SIGMETRICS (International Conference on Measurement and Modeling of Computer Systems), Annapolis, MD, June 2008.
41. A Scratch-Pad Memory Aware Dynamic Loop Scheduling Algorithm, by O. Ozturk, M. Kandemir, and S. H. K. Narayanan. In Proc. the 9th International Symposium on Quality Electronic Design (ISQED'08), San Jose, CA, March 2008.
42. An ILP Based Approach to Reducing Energy Consumption in NoC Based CMPs, by O. Ozturk, M. Kandemir, and S. W. Son. In Proc. of the International Symposium on Low Power Electronics and Design (ISLPED'07), pp. 411-414, Portland, OR, Aug 2007.
43. A Memory-Conscious Code Parallelization Scheme, by L. Xue, O. Ozturk, and M. Kandemir. In Proc. of the 44th Design Automation Conference (DAC'07); June 2007; San Diego, CA.

44. Reducing Off-Chip Memory Access Costs Using Data Recomputation in Embedded Chip Multi-processors; by H. Koc, M. Kandemir, E. Ercanli, O. Ozturk; In Proc. of the 44th Design Automation Conference (DAC'07); June 2007; San Diego, CA.
45. Memory Bank Aware Dynamic Loop Scheduling by M. Kandemir, T. Yemliha, S. W. Son, and O. Ozturk. In Proc. of Design, Automation and Test in Europe (DATE'07), Nice, France, April 2007.
46. Compiler-Directed Variable Latency Aware SPM Management to Cope With Timing Problems, by O. Ozturk, M. Kandemir, and M. Karakoy. In Proc. IEEE/ACM International Symposium on Code Generation and Optimization (CGO'07), San Jose, CA, March 2007.
47. An ILP Formulation for Recomputation Based SPM Management for Embedded CMPs; by Hakduran Koc, Ehat Ercanli, Mahmut T. Kandemir, Ozcan Ozturk; In Proceedings of the 5th Workshop on Optimizations for DSP and Embedded Systems (ODES'07); March 2007; San Jose, CA.
48. Enhancing Locality in Two-Dimensional Space through Integrated Computation and Data Mappings, by M. Kandemir, O. Ozturk, and V. S. Degalahal. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
49. A Process Scheduler-Based Approach to NoC Power Management, by F. Li, G. Chen, M. Kandemir, O. Ozturk, M. Karakoy, R. Ramanarayanan, and B. Vaidyanathan. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
50. Compiler-Directed Code Restructuring for Operating with Compressed Arrays, by T. Yemliha, G. Chen, O. Ozturk, M. Kandemir, and V. S. Degalahal. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
51. Locality-Aware Distributed Loop Scheduling For Chip Multiprocessors, by L. Xue, M. Kandemir, G. Chen, F. Li, O. Ozturk, R. Ramanarayanan, and B. Vaidyanathan. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
52. Cache miss clustering for banked memory systems, by O. Ozturk, G. Chen, M. Kandemir, and M. Karakoy. In Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD'06), San Jose, CA, November 2006.
53. Minimizing energy consumption of banked memories using data recomputation, by H. Koc, O. Ozturk, M. Kandemir, S. H. K. Narayanan, and E. Ercanli. In Proc. International Symposium on Low Power Electronics and Design (ISLPED'06), Tegernsee, Germany, October 2006.
54. Energy-aware code replication for improving reliability in embedded chip multiprocessors, by G. Chen, O. Ozturk, and M. Kandemir. In Proc. IEEE International SOC Conference (SOCC'06), Austin, TX, September 2006.
55. A Constraint Network Based Solution to Code Parallelization, by O. Ozturk, G. Chen, and M. Kandemir. In Proc. Design Automation Conference (DAC'06), San Francisco, CA, July 2006. **(Best Paper Candidate)**
56. Multi-level On-chip Memory Hierarchy Design for Embedded Chip Multiprocessors, by O. Ozturk, M. Kandemir, M. J. Irwin, and S. Tosun. In Proc. The Twelfth International Conference on Parallel and Distributed Systems (ICPADS'06), July 2006. **(Best Paper Award)**
57. Selective Code/Data Migration for Reducing Communication Energy in Embedded MpSoC Architectures, by O. Ozturk, M. Kandemir, and M. Karakoy. In Proc. GLSVLSI, Philadelphia, PA, May 2006.
58. An ILP Based Approach to Address Code Generation for Digital Signal Processors, by O. Ozturk, M. Kandemir, and S. Tosun. In Proc. GLSVLSI, Philadelphia, PA, May 2006.
59. Multi-compilation: capturing interactions among concurrently-executing applications, by O. Ozturk, G. Chen, and M. Kandemir. In Proc. ACM International Conference on Computing Frontiers, Ischia, Italy, May 2006.
60. ILP-Based Management of Multi-Level Memory Hierarchies, by O. Ozturk, M. Kandemir, and S. W. Son. In Proc. 4th Workshop on Optimizations for DSP and Embedded Systems (ODES'06), Manhattan, New York, NY, March, 2006.
61. Managing SPM Space Based on Inter-Application Data Sharing, by O. Ozturk, M. Kandemir, S. W. Son, and I. Kolcu. In Proc. 4th Workshop on Optimizations for DSP and Embedded Systems (ODES'06), Manhattan, New York, NY, March, 2006.
62. Dynamic Scratch-Pad Memory Management for Irregular Array Access Patterns, by G. Chen, O. Ozturk, M. Kandemir, and M. Karakoy. Design Automation and Test in Europe (DATE'06), Munich, Germany, March 2006.
63. Dynamic Partitioning of Processing and Memory Resources in Embedded MPSoC Architectures, by L. Xue, O. Ozturk, F. Li, and I. Kolcu. Design Automation and Test in Europe (DATE'06), Munich, Germany, March 2006.
64. Data Replication in Banked DRAMs for Reducing Energy Consumption, by O. Ozturk and M. Kandemir. In Proc. the 7th International Symposium on Quality Electronic Design (ISQED'06), San Jose, CA, March 2006.
65. Shared Scratch-Pad Memory Space Management, by O. Ozturk, M. Kandemir, and I. Kolcu. In Proc. the 7th International Symposium on Quality Electronic Design (ISQED'06), San Jose, CA, March 2006.
66. Compiler-Directed Power Density Reduction in NoC-Based Multi-Core Designs, by S. H. K. Narayanan, O. Ozturk, and M. Kandemir. In Proc. the 7th International Symposium on Quality Electronic Design (ISQED'06), San Jose, CA, March 2006.
67. An Integer Linear Programming Based Approach to Simultaneous Memory Space Partitioning and Data Allocation for Chip Multiprocessors, by O. Ozturk, G. Chen, M. Kandemir, and M. Karakoy. In Proc. IEEE Computer Society Annual Symposium on VLSI 2006 (ISVLSI 2006), Karlsruhe, Germany, March, 2006.
68. Task Recomputation in Memory Constrained Embedded Multi-CPU Systems, by H. Koc, S. Tosun, O. Ozturk, and M. Kandemir. In Proc. IEEE Computer Society Annual Symposium on VLSI 2006 (ISVLSI 2006), Karlsruhe, Germany, March, 2006.
69. Leakage-Aware SPM Management, by G. Chen, F. Li, O. Ozturk, G. Chen, M. Kandemir, and I. Kolcu. In Proc. IEEE Computer Society Annual Symposium on VLSI 2006 (ISVLSI 2006), Karlsruhe, Germany, March, 2006.

70. Compiler-Guided Data Compression for Reducing Memory Consumption of Embedded Applications, by O.Ozturk, G.Chen, M.Kandemir. In Proc. the Asia and South Pacific Design Automation Conference (ASPDAC'06), Yokohama, Japan, January 2006.
71. Optimal Topology Exploration for Application-Specific 3D Architectures, by O.Ozturk, F.Wang, M.Kandemir, Y.Xie. In Proc. the Asia and South Pacific Design Automation Conference (ASPDAC'06), Yokohama, Japan, January 2006.
72. Integrating Loop and Data Optimizations for Locality within a Constraint Network Based Framework, by G.Chen, O.Ozturk, M.Kandemir, and I.Kolcu. In Proc. International Conference on Computer Aided Design (ICCAD'05), San Jose, CA, November 2005.
73. Increasing On-Chip Memory Space Utilization for Embedded Chip Multiprocessors through Data Compression. O.Ozturk, M.Kandemir, M.J.Irwin. In Proc. IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'05), New York, September 2005.
74. On-Chip Memory Management for Embedded MpSoC Architectures Based on Data Compression. O.Ozturk, M.Kandemir, M.J.Irwin. In Proc. IEEE International SOC Conference (SOCC 2005), Washington, D.C., September 2005.
75. Workload Clustering for Increasing Energy Savings on Embedded MPSoCs, S.H.K.Narayan, O.Ozturk, M.Kandemir, M.Karakoy. In Proc. IEEE International SOC Conference (SOCC 2005), Washington, D.C., September 2005.
76. Constraint-Based Code Mapping for Heterogeneous Chip Multiprocessors, S. Tosun, N. Mansouri, M. Kandemir, O. Ozturk. In Proc. IEEE International SOC Conference (SOCC 2005), Washington, D.C., September 2005.
77. Exploiting Inter-Processor Data Sharing for Improving Behavior of Multi-Processor SoCs, by G.Chen, G.Chen, O.Ozturk, and M.Kandemir. In Proc. IEEE Computer Society Annual Symposium on VLSI 2005 (ISVLSI 2005), Tampa, Florida, May 11-12, 2005.
78. A Data-Driven Approach for Embedded Security, by H.Saputra, O.Ozturk, N.Vijaykrishnan, M.Kandemir, and R.Brooks. In Proc. IEEE Computer Society Annual Symposium on VLSI 2005 (ISVLSI 2005), Tampa, Florida, May 11-12, 2005.
79. Energy management in software-controlled multi-level memory hierarchies, by O.Ozturk and M.Kandemir. In Proc. GLSVLSI'05, Chicago, IL, April 2005.
80. Integer linear programming based energy optimization for banked DRAMs, by O.Ozturk and M.Kandemir. In Proc. GLSVLSI'05, Chicago, IL, April 2005.
81. Using data compression in an MPSoC architecture for improving performance, by O.Ozturk, M.Kandemir, and M.J.Irwin. In Proc. GLSVLSI'05, Chicago, IL, April 2005.
82. Access pattern-based code compression for memory-constrained embedded systems, by O.Ozturk, H.Saputra, M.Kandemir, and I.Kolcu. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
83. BB-GC: basic-block level garbage collection, by O.Ozturk, M.Kandemir and M.J.Irwin. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
84. Nonuniform banking for reducing memory energy consumption, by O.Ozturk and M.Kandemir. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
85. Increasing register file immunity to transient errors, by G.Memik, M.Kandemir, and O.Ozturk. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
86. Studying storage-recomputation tradeoffs in memory-constrained embedded processing, by M.Kandemir, F.Li, G.Chen, G.Chen, and O.Ozturk. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
87. An ILP formulation for reliability-oriented high-level synthesis, by S.Tosun, O.Ozturk, N.Mansouri, E.Arvas, M.Kandemir, and Y.Xie. In Proc. the 6th International Symposium on Quality Electronic Design (ISQED'05), San Jose, CA, March 2005.
88. An adaptive locality-conscious process scheduler for embedded systems, by G.Chen, G.Chen, O.Ozturk, and M.Kandemir. In Proc. 11th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'05), San Francisco, California, March 2005.
89. Customized on-chip memories for embedded chip multiprocessors, by O.Ozturk, M.Kandemir, G.Chen, M.J.Irwin, and M.Karakoy. In Proc. the Asia and South Pacific Design Automation Conference (ASPDAC'05), Shanghai, China, January 2005.
90. Dynamic on-chip memory management for chip multiprocessors, by M.Kandemir, O.Ozturk, and M.Karakoy. In Proc. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES'04), Washington D.C., September 2004.
91. Data compression for improving SPM behavior, by O.Ozturk, M.Kandemir, I.Demirkiran, G.Chen, and M.J.Irwin. In Proc. the 41st Design Automation Conference (DAC'04), San Diego, CA, June 2004. **(Best Paper Candidate)**
92. Tuning data replication for improving behavior of MPSoC applications, by O.Ozturk, M.Kandemir, M.J.Irwin, and I.Kolcu. In Proc. the 2004 Great Lakes Symposium on VLSI (GLSVLSI'04), Boston, MA, April 26-28, 2004.

PRESENTATIONS

1. AutopaR: An Automatic Parallelization Tool for Recursive Calls, The Fifth International Workshop on Parallel Software Tools and Tool Infrastructures (PSTI 2014), Minneapolis, MN, September, 2014.
2. Adaptive Compute-phase Prediction and Thread Prioritization to Mitigate Memory Access Latency, International Workshop on Manycore Embedded Systems, June 2014, Minneapolis, MN.
3. Staggered Latch Bus: A Reliable Offset Switched Architecture for Long On-Chip Interconnect, 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Istanbul, Turkey, October 2013.
4. Effective Kernel Mapping for OpenCL Applications in Heterogeneous Platforms, *International Conference on Parallel Processing, Pittsburgh, PA, USA, September 2012.*
5. Reliability-Aware 3D Chip Multiprocessor Design, *Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'12), Annecy, France, June 2012.*
6. Manycore Processors and Parallel Programming, *Invited Speaker, National High Performance Computing Conference, Ankara, Nisan 2012.*
7. Optimizing Parallel Behavior of OpenFOAM, *Stanford University, Stanford, CA, May 2011.*
8. Cache-Aware Application and Thread Scheduling, *NEC Labs, Princeton, NJ, June 2011.*
9. Multicore Education Through Simulation, *Microelectronic Systems Education (MSE'09), San Francisco, CA, July 2009.*
10. Compiler Optimizations for Chip Multiprocessors, *Munich, Germany, May 2009, HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation)*
11. Compiler-Guided Optimizations for Memory-Constrained Embedded Systems, *Koç University, Istanbul, April 2007.*
12. Memory Hierarchy Design For Chip Multiprocessors - A Compiler Directed Approach, *Bilkent University, April 2007.*
13. Enhancing Locality In Two-Dimensional Space Through Integrated Computation And Data Mappings *VLSI Design Conference 2007, Bangalore, India, January 2007.*
14. A Process Scheduler-Based Approach to NoC Power Management *VLSI Design Conference 2007, Bangalore, India, January 2007.*
15. Locality-Aware Distributed Loop Scheduling For Chip Multiprocessors *VLSI Design Conference 2007, Bangalore, India, January 2007.*
16. Cache miss clustering for banked memory systems *VLSI Design Conference 2007, Bangalore, India, January 2007.*
17. Cache miss clustering for banked memory systems *ICCAD 2006, San Jose, CA, November 2006.*
18. Multi-level On-chip Memory Hierarchy Design for Embedded Chip Multiprocessors *ICPADS 2006, Minneapolis, MN, June 2006.*
19. Selective Code/Data Migration for Reducing Communication Energy in Embedded MpSoC Architectures
20. An ILP Based Approach to Address Code Generation for Digital Signal Processors *GLSVLSI 2006, Philadelphia, PA, April 2006.*
21. Managing SPM Space Based on Inter-Application Data Sharing *ODES-4, Manhattan, New York, March 2006.*
22. Dynamic Scratch-Pad Memory Management for Irregular Array Access Patterns *DATE 2006, Munich, Germany, March 2006.*
23. Dynamic Partitioning of Processing and Memory Resources in Embedded MPSoC Architectures *DATE 2006, Munich, Germany, March 2006.*
24. M-Opt: Memory Design Optimizer tool demonstration *GSRC Quarterly Workshop, Berkeley, CA, March 2006.*
25. Shared Scratch-Pad Memory Space Management *ISQED 2006, San Jose, CA, March 2006.*
26. An Integer Linear Programming Based Approach to Simultaneous Memory Space Partitioning and Data Allocation for Chip Multiprocessors *ISVLSI 2006, Karlsruhe, Germany, March 2006.*
27. Task Recomputation in Memory Constrained Embedded Multi-CPU Systems *ISVLSI 2006, Karlsruhe, Germany, March 2006.*
28. Leakage-Aware SPM Management *ISVLSI 2006, Karlsruhe, Germany, March 2006.*
29. On-Chip Memory Management for Embedded MpSoC Architectures Based on Data Compression *SOCC 2005, Washington, DC, September 2005.*
30. Workload Clustering for Increasing Energy Savings on Embedded MPSoCs *SOCC 2005, Washington, DC, September 2005.*
31. Automatic Memory Partitioning: *GSRC Quarterly Workshop, Anaheim, CA, June 2005*

32. Exploiting Inter-Processor Data Sharing for Improving Behavior of Multi-Processor SoCs:
ISVLSI 2005, Tampa, Florida, May 2005
33. Access Pattern-Based Code Compression for Memory-Constrained Embedded Systems
DATE 2005, Munich, Germany, March 2005.
34. BB-GC: Basic-Block Level Garbage Collection
DATE 2005, Munich, Germany, March 2005.
35. Nonuniform Banking for Reducing Memory Energy Consumption
DATE 2005, Munich, Germany, March 2005.
36. Increasing Register File Immunity to Transient Errors
DATE 2005, Munich, Germany, March 2005.
37. Reliability-Centric High-Level Synthesis
DATE 2005, Munich, Germany, March 2005.
38. Dynamic On-Chip Memory Management for Chip Multiprocessors
CASES 2004, Washington D.C., September 2004