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EDUCATION

Ph.D. in Computer Science and Engineering, May 2007
The Pennsylvania State University, University Park, PA.

Master of Science in Computer and Information Science and Engineering, August 2002
University of Florida, Gainesville, FL.

Bachelor of Science in Computer Engineering, June 2000
Bogazici University, Istanbul, Turkey

INDUSTRIAL AND ACADEMIC EXPERIENCE

- **Assistant Professor, Bilkent University**, Computer Engineering Department, Ankara, Turkey, January 2008 – Present.
- **Visiting Researcher, INRIA**, Paris, France, June 2009 – August 2009, ALCHEMY group (Architectures, Languages and Compilers to Harness the End of Moore Years): Optimization using Polyhedral Model.
- **Consultant**, Erendiz Supercomputer, Eskisehir, Turkey, 2008 - 2009
- **Senior Software Optimization Engineer, Intel Corporation**, Cellular and Handheld Group - Marvell, April 2006 – January 2008, Chandler, Arizona: Senior Software Optimization Engineer.
- **Research Associate**, Processor Architecture Laboratory (LAP), **Swiss Federal Institute of Technology of Lausanne (EPFL)**, July 2003 – August 2003, Lausanne, Switzerland: Optimization of a MachSUIF compiler backend for the ARM architecture.
- **Research Assistant/Teaching Assistant**, CSE Department, August 2002 – August 2006, Pennsylvania State University, State College, Pennsylvania.
- **Teaching Assistant**, Computer and Information Science and Engineering Department, August 2000 – May 2002, University of Florida, Gainesville, Florida.

HONORS/AWARDS

- IBM Faculty Award, 2009.
- EC FP7 HPC-Europa2 Transnational Access Programme Grant
- European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) Paper Award, 2009.
- Tubitak (Turkish NSF) Award for European Union FP7 Marie Curie IRG project acceptance, 2009.
- The most popular paper from ACM's refereed journals and conference proceedings downloaded, October 2006 (Communications of the ACM, January 2007/Vol. 50, No. 1).
- Best Paper Award from the Twelfth International Conference on Parallel and Distributed Systems (ICPADS'06), Minneapolis, Minnesota, June 2006.
- Nominated for Best Paper Award in DAC-2006, San Francisco, CA, July 2006.
- Selected for Marquis Who's Who in America, 2006-2007.
- Selected by SIGDA to present at the PhD Forum of DAC-2005, Anaheim, CA, June 2005.
- Selected by European Design Automation Association (EDAA) to present at the PhD Forum of DATE-2005, Munich, Germany, March 2005.
- Nominated for Best Paper Award in DAC-2004, San Diego, CA, June 2004.
- Young Student Support Program Award in Design Automation Conference, San Diego, June, 2004.
- Scholarship from Swiss Federal Institute of Technology of Lausanne (EPFL), July 2003.
- Ranked in top 300 in Nationwide University Exam (OYS) among 1.3 million, Turkey, 1996.

RESEARCH INTERESTS

Computer Architecture, On-Chip Multiprocessing, Power-Aware Architectures, Compiler Optimizations, and Programming Languages

RESEARCH PROJECTS

- Heterogeneous Chip Multiprocessor Design (HTCMP), Funded by European Commission (EC) FP7-PEOPLE MARIE CURIE ACTIONS, 2009 – 2013, €100,000.
- Energy Efficient Application Mapping onto Network-on-Chips with Different Topologies, Funded by The Scientific & Technological Council of Turkey (TUBITAK – 108E233), 2009 – 2012, (with Asst. Prof. Suleyman Tosun, Ankara University).

PROFESSIONAL ACTIVITIES

- HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation) member.
- GSRC (Gigascale Systems Research Center) member.
- IEEE and ACM member.
- Editorial Board Member, International Journal of Computer Science and Software Technology (IJCSST), International Science Press.
- Editorial Board Member, Journal of Computer Science and Information Technology (JCSIT).
- Program Committee Member
 - NSS 2009 - 3rd International Conference on Network and System Security
 - DSD 2009 - 12th Euromicro Conference on Digital System Design
 - ISCIS 2009 - 24th International Symposium on Computer and Information Sciences
 - TTSDP 2009 - Tools and Techniques in Software Development Processes for High Performance computing
 - SMM 2009 - Software Metrics and Measurement
 - SEPA 2009 - Software Engineering Processes and Applications
- Refereeing for Scholarly and Professional Journals
 - IEEE Transactions on Parallel and Distributed Systems
 - IEEE Transactions on Computer Aided Design
 - IEEE Signal Processing Magazine
 - IEEE Transactions on Very Large Scale Integration (VLSI) Systems
 - ACM Transactions on Design Automation of Electronic Systems
 - ACM Transactions on Embedded Computing Systems
 - ACM Transactions on Architecture and Code Optimization
 - Elsevier Computer Communications
 - Wiley Concurrency and Computation: Practice and Experience
 - Journal of Computer Science and Technology
- Reviewer for several conferences: PACT, EMSOFT, ICCD, CASES, DATE, ISLPED, ISPASS, ISCAS, TVLSI, TODAES, TCAD, Computer Architecture Letters, HiPC, etc.

TEACHING INTERESTS

- CS 423 – Computer Architecture (Fall 09)
- CS 541 – Chip Multiprocessors (Spring 08, Spring 09)
- CS 590/690 – Research Topics (Fall 08)
- CS 224 – Computer Organization (Spring 08, Spring 09)
- CS 223 – Digital Design (Fall 08)
- CS 102 – Algorithms and Programming II (Summer 08)

PUBLICATIONS

Books:

Memory Hierarchy Design For Chip Multiprocessors: A Compiler Directed Approach (Paperback) by Ozcan Ozturk, VDM Verlag Dr. Müller, December, 2008.

Journals:

1. Using Data Compression for Increasing Memory System Utilization, by Ozcan Ozturk, Mahmut Kandemir, Mary J. Irwin. IEEE Transactions on Computer Aided Design, Volume 28, Number 6, pages 901-914, June 2009.
2. Shared scratch pad memory space management across applications, by O. Ozturk, M. Kandemir, S. W. Son, and I. Kolcu. International Journal of Embedded Systems, Vol. 4, No.1 pp. 54 – 65, 2009.
3. ILP Based Energy Minimization Techniques for Banked Memories, by O. Ozturk and M. Kandemir. ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13 , Issue 3, July 2008.
4. Access Pattern-Based Code Compression For Memory-Constrained Systems, by O. Ozturk, M. Kandemir, and G. Chen. ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13, Issue 4, September 2008.
5. Basic-Block Level Garbage Collection for Memory-Limited Embedded Systems, by Ozcan Ozturk, Mahmut Kandemir, Mary J. Irwin. To appear in International Journal of Embedded Systems.
6. Compiler-Directed Energy Optimization for Parallel Disk Based Systems, by S. W. Son, G. Chen, O. Ozturk, M. Kandemir, and A. Choudhary, IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 18, Number 9, pp. 1241-1257, September, 2007.
7. Optimizing Array-Intensive Applications for On-Chip Multiprocessors, by I.Kadayif, M.Kandemir, G.Chen, O.Ozturk, M.Karakoy, and U.Sezer. IEEE Transactions on Parallel and Distributed Systems (TPDS), Volume 16, Number 5, May 2005.
8. An ILP formulation for task scheduling on heterogeneous chip multiprocessors, by S. Tosun, N. Mansouri, and M. Kandemir. Lecture Notes in Computer Science (LNCS) 4263 Springer 2006, ISBN 3-540-47242-8.
9. An ILP-Based Approach to Locality Optimization, by G. Chen, O. Ozturk, and M. Kandemir. Lecture Notes in Computer Science (LNCS) 3602 Springer 2004, Languages and Compilers for High Performance Computing, pages 149-163.
10. Using data compression to increase energy savings in multi-bank memories, by M.Kandemir, O.Ozturk, M.J.Irwin, and I.Kolcu. Lecture Notes in Computer Science (LNCS) 3149 Springer 2004, ISBN 3-540-22924-8, pages 310-317.

Conferences:

1. Optimizing Shared Cache Behavior of Chip Multiprocessors, by M. Kandemir, S.P.Muralidhara, S. Narayanan, Y. Zhang, and O. Ozturk. In Proc. of The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'09), New York City, NY, December 2009.
2. Slicing Based Code Parallelization for Minimizing Interprocessor Communication, by M. Kandemir, Y. Zhang, S. P. Muralidhara, O. Ozturk and S. Narayanan. In Proc. of CASES'09, Grenoble, France, October 2009.
3. Optimizing Scratch-Pad Memory Allocation and Assignment Through a Decoupled Approach, Boubacar Diouf, Ozcan Ozturk, and Albert Cohen. In Proc. of the 22nd International Workshop on Languages and Compilers for Parallel Computing (LCPC'09), October 2009, Newark, Delaware.
4. An ILP Formulation for Application Mapping onto Network-on-Chips, by S. Tosun, O. Ozturk, M. Ozen. In Proc. of The 3rd IEEE International Conference on Application of Information and Communication Technologies (AICT'09), Baku, Azerbaijan, October 2009.
5. Multicore Education Through Simulation, Ozcan Ozturk. In Proc. Of Microelectronic Systems Education (MSE'09), July 2009, San Francisco, CA.
6. Dynamic Thread and Data Mapping for NoC Based CMPs, Mahmut Kandemir, Ozcan Ozturk, and S.P.Muralidhara. In Proc. of 46th Design Automation Conference (DAC'09), July 2009, San Francisco, CA.
7. Heterogeneous Chip Multiprocessor Design, Ozcan Ozturk. Designing for embedded parallel computing platforms: architectures, tools, and applications Workshop, Design, Automation and Test in Europe (DATE'09).
8. Using Dynamic Compilation for Continuing Execution Under Reduced Memory Availability, Ozcan Ozturk, Mahmut Kandemir. In Proc. of Design, Automation and Test in Europe (DATE'09), Nice, France, April 2009.
9. Adaptive Prefetching for Shared Cache Based Chip Multiprocessors, Mahmut Kandemir, Yuanrui Zhang, Ozcan Ozturk. In Proc. of Design, Automation and Test in Europe (DATE'09), Nice, France, April 2009.
10. Process Variation Aware Thread Mapping For Chip Multiprocessors by S Hong, S H K Narayanan, and M Kandemir, O Ozturk. In Proc. of Design, Automation and Test in Europe (DATE'09), Nice, France, April 2009.
11. SPM Management Using Markov Chain Based Data Access Prediction, by T. Yemliha, S. Srikantiah, M. Kandemir, and O. Ozturk. In Proc. International Conference on Computer Aided Design (ICCAD'08), San Jose, CA, November 2008.
12. Prefetch Throttling and Data Pinning for Improving Performance of Shared Caches by O. Ozturk, S. W. Son, M. Kandemir, and M. Karakoy. To appear in Proc. of the ACM/IEEE Conference on High Performance Networking and Computing (SC'08), Austin, TX, Nov 2008.
13. Profiler and Compiler Assisted Adaptive I/O Prefetching for Shared Storage Caches, by S. W. Son, S. P. Muralidhara, O. Ozturk, M. Kandemir, I. Kolcu, and M. Karakoy. In Proc. International Conference on Parallel Architecture and Compilation Techniques PACT-2008 Toronto , Canada October 25-29, 2008.

14. Software-Directed Combined CPU/Link Voltage Scaling for NoC-Based CMPs, by O. Ozturk and M. Kandemir. In Proc. the ACM SIGMETRICS (International Conference on Measurement and Modeling of Computer Systems), Annapolis, MD, June 2008.
15. A Scratch-Pad Memory Aware Dynamic Loop Scheduling Algorithm, by O. Ozturk, M. Kandemir, and S. H. K. Narayanan. In Proc. the 9th International Symposium on Quality Electronic Design (ISQED'08), San Jose, CA, March 2008.
16. An ILP Based Approach to Reducing Energy Consumption in NoC Based CMPs, by O. Ozturk, M. Kandemir, and S. W. Son. In Proc. of the International Symposium on Low Power Electronics and Design (ISLPED'07), pp. 411-414, Portland, OR, Aug 2007.
17. A Memory-Conscious Code Parallelization Scheme, by L. Xue, O. Ozturk, and M. Kandemir. In Proc. of the 44th Design Automation Conference (DAC'07); June 2007; San Diego, CA.
18. Reducing Off-Chip Memory Access Costs Using Data Recomputation in Embedded Chip Multi-processors; by H. Koc, M. Kandemir, E. Ercanli, O. Ozturk; In Proc. of the 44th Design Automation Conference (DAC'07); June 2007; San Diego, CA.
19. Memory Bank Aware Dynamic Loop Scheduling by M. Kandemir, T. Yemliha, S. W. Son, and O. Ozturk. In Proc. of Design, Automation and Test in Europe (DATE'07), Nice, France, April 2007.
20. Compiler-Directed Variable Latency Aware SPM Management to Cope With Timing Problems, by O. Ozturk, M. Kandemir, and M. Karakoy. In Proc. IEEE/ACM International Symposium on Code Generation and Optimization (CGO'07), San Jose, CA, March 2007.
21. An ILP Formulation for Recomputation Based SPM Management for Embedded CMPs; by Hakduran Koc, Ehat Ercanli, Mahmut T. Kandemir, Ozcan Ozturk; In Proceedings of the 5th Workshop on Optimizations for DSP and Embedded Systems (ODES'07); March 2007; San Jose, CA.
22. Enhancing Locality in Two-Dimensional Space through Integrated Computation and Data Mappings, by M. Kandemir, O. Ozturk, and V. S. Degalahal. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
23. A Process Scheduler-Based Approach to NoC Power Management, by F. Li, G. Chen, M. Kandemir, O. Ozturk, M. Karakoy, R. Ramanarayanan, and B. Vaidyanathan. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
24. Compiler-Directed Code Restructuring for Operating with Compressed Arrays, by T. Yemliha, G. Chen, O. Ozturk, M. Kandemir, and V. S. Degalahal. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
25. Locality-Aware Distributed Loop Scheduling For Chip Multiprocessors, by L. Xue, M. Kandemir, G. Chen, F. Li, O. Ozturk, R. Ramanarayanan, and B. Vaidyanathan. In Proc. 20th International Conference on VLSI Design (VLSI'07), Bangalore, India, January 2007.
26. Cache miss clustering for banked memory systems, by O. Ozturk, G. Chen, M. Kandemir, and M. Karakoy. In Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD'06), San Jose, CA, November 2006.
27. Minimizing energy consumption of banked memories using data recomputation, by H. Koc, O. Ozturk, M. Kandemir, S. H. K. Narayanan, and E. Ercanli. In Proc. International Symposium on Low Power Electronics and Design (ISLPED'06), Tegernsee, Germany, October 2006.
28. Energy-aware code replication for improving reliability in embedded chip multiprocessors, by G. Chen, O. Ozturk, and M. Kandemir. In Proc. IEEE International SOC Conference (SOCC'06), Austin, TX, September 2006.
29. A Constraint Network Based Solution to Code Parallelization, by O. Ozturk, G. Chen, and M. Kandemir. In Proc. Design Automation Conference (DAC'06), San Francisco, CA, July 2006. **(Best Paper Candidate)**
30. Multi-level On-chip Memory Hierarchy Design for Embedded Chip Multiprocessors, by O. Ozturk, M. Kandemir, M. J. Irwin, and S. Tosun. In Proc. The Twelfth International Conference on Parallel and Distributed Systems (ICPADS'06), July 2006. **(Best Paper Award)**
31. Selective Code/Data Migration for Reducing Communication Energy in Embedded MpSoC Architectures, by O. Ozturk, M. Kandemir, and M. Karakoy. In Proc. GLSVLSI, Philadelphia, PA, May 2006.
32. An ILP Based Approach to Address Code Generation for Digital Signal Processors, by O. Ozturk, M. Kandemir, and S. Tosun. In Proc. GLSVLSI, Philadelphia, PA, May 2006.
33. Multi-compilation: capturing interactions among concurrently-executing applications, by O. Ozturk, G. Chen, and M. Kandemir. In Proc. ACM International Conference on Computing Frontiers, Ischia, Italy, May 2006.
34. ILP-Based Management of Multi-Level Memory Hierarchies, by O. Ozturk, M. Kandemir, and S. W. Son. In Proc. 4th Workshop on Optimizations for DSP and Embedded Systems (ODES'06), Manhattan, New York, NY, March, 2006.
35. Managing SPM Space Based on Inter-Application Data Sharing, by O. Ozturk, M. Kandemir, S. W. Son, and I. Kolcu. In Proc. 4th Workshop on Optimizations for DSP and Embedded Systems (ODES'06), Manhattan, New York, NY, March, 2006.
36. Dynamic Scratch-Pad Memory Management for Irregular Array Access Patterns, by G. Chen, O. Ozturk, M. Kandemir, and M. Karakoy. Design Automation and Test in Europe (DATE'06), Munich, Germany, March 2006.
37. Dynamic Partitioning of Processing and Memory Resources in Embedded MPSoC Architectures, by L. Xue, O. Ozturk, F. Li, and I. Kolcu. Design Automation and Test in Europe (DATE'06), Munich, Germany, March 2006.
38. Data Replication in Banked DRAMs for Reducing Energy Consumption, by O. Ozturk and M. Kandemir. In Proc. the 7th International Symposium on Quality Electronic Design (ISQED'06), San Jose, CA, March 2006.
39. Shared Scratch-Pad Memory Space Management, by O. Ozturk, M. Kandemir, and I. Kolcu. In Proc. the 7th International Symposium on Quality Electronic Design (ISQED'06), San Jose, CA, March 2006.

40. Compiler-Directed Power Density Reduction in NoC-Based Multi-Core Designs, by S. H. K. Narayanan, O. Ozturk, and M. Kandemir. In Proc. the 7th International Symposium on Quality Electronic Design (ISQED'06), San Jose, CA, March 2006.
41. An Integer Linear Programming Based Approach to Simultaneous Memory Space Partitioning and Data Allocation for Chip Multiprocessors, by O. Ozturk, G. Chen, M. Kandemir, and M. Karakoy. In Proc. IEEE Computer Society Annual Symposium on VLSI 2006 (ISVLSI 2006), Karlsruhe, Germany, March, 2006.
42. Task Recomputation in Memory Constrained Embedded Multi-CPU Systems, by H. Koc, S. Tosun, O. Ozturk, and M. Kandemir. In Proc. IEEE Computer Society Annual Symposium on VLSI 2006 (ISVLSI 2006), Karlsruhe, Germany, March, 2006.
43. Leakage-Aware SPM Management, by G. Chen, F. Li, O. Ozturk, G. Chen, M. Kandemir, and I. Kolcu. In Proc. IEEE Computer Society Annual Symposium on VLSI 2006 (ISVLSI 2006), Karlsruhe, Germany, March, 2006.
44. Compiler-Guided Data Compression for Reducing Memory Consumption of Embedded Applications, by O.Ozturk, G.Chen, M.Kandemir. In Proc. the Asia and South Pacific Design Automation Conference (ASPDAC'06), Yokohama, Japan, January 2006.
45. Optimal Topology Exploration for Application-Specific 3D Architectures, by O.Ozturk, F.Wang, M.Kandemir, Y.Xie. In Proc. the Asia and South Pacific Design Automation Conference (ASPDAC'06), Yokohama, Japan, January 2006.
46. Integrating Loop and Data Optimizations for Locality within a Constraint Network Based Framework, by G.Chen, O.Ozturk, M.Kandemir, and I.Kolcu. In Proc. International Conference on Computer Aided Design (ICCAD'05), San Jose, CA, November 2005.
47. Increasing On-Chip Memory Space Utilization for Embedded Chip Multiprocessors through Data Compression. O.Ozturk, M.Kandemir, M.J.Irwin. In Proc. IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'05), New York, September 2005.
48. On-Chip Memory Management for Embedded MpSoC Architectures Based on Data Compression. O.Ozturk, M.Kandemir, M.J.Irwin. In Proc. IEEE International SOC Conference (SOCC 2005), Washington, D.C., September 2005.
49. Workload Clustering for Increasing Energy Savings on Embedded MPSoCs, S.H.K.Narayan, O.Ozturk, M.Kandemir, M.Karakoy. In Proc. IEEE International SOC Conference (SOCC 2005), Washington, D.C., September 2005.
50. Constraint-Based Code Mapping for Heterogeneous Chip Multiprocessors, S. Tosun, N. Mansouri, M. Kandemir, O. Ozturk. In Proc. IEEE International SOC Conference (SOCC 2005), Washington, D.C., September 2005.
51. Exploiting Inter-Processor Data Sharing for Improving Behavior of Multi-Processor SoCs, by G.Chen, G.Chen, O.Ozturk, and M.Kandemir. In Proc. IEEE Computer Society Annual Symposium on VLSI 2005 (ISVLSI 2005), Tampa, Florida, May 11-12, 2005.
52. A Data-Driven Approach for Embedded Security, by H.Saputra, O.Ozturk, N.Vijaykrishnan, M.Kandemir, and R.Brooks. In Proc. IEEE Computer Society Annual Symposium on VLSI 2005 (ISVLSI 2005), Tampa, Florida, May 11-12, 2005.
53. Energy management in software-controlled multi-level memory hierarchies, by O.Ozturk and M.Kandemir. In Proc. GLSVLSI'05, Chicago, IL, April 2005.
54. Integer linear programming based energy optimization for banked DRAMs, by O.Ozturk and M.Kandemir. In Proc. GLSVLSI'05, Chicago, IL, April 2005.
55. Using data compression in an MPSoC architecture for improving performance, by O.Ozturk, M.Kandemir, and M.J.Irwin. In Proc. GLSVLSI'05, Chicago, IL, April 2005.
56. Access pattern-based code compression for memory-constrained embedded systems, by O.Ozturk, H.Saputra, M.Kandemir, and I.Kolcu. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
57. BB-GC: basic-block level garbage collection, by O.Ozturk, M.Kandemir and M.J.Irwin. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
58. Nonuniform banking for reducing memory energy consumption, by O.Ozturk and M.Kandemir. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
59. Increasing register file immunity to transient errors, by G.Memik, M.Kandemir, and O.Ozturk. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
60. Studying storage-recomputation tradeoffs in memory-constrained embedded processing, by M.Kandemir, F.Li, G.Chen, G.Chen, and O.Ozturk. In Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, March 2005.
61. An ILP formulation for reliability-oriented high-level synthesis, by S.Tosun, O.Ozturk, N.Mansouri, E.Arvas, M.Kandemir, and Y.Xie. In Proc. the 6th International Symposium on Quality Electronic Design (ISQED'05), San Jose, CA, March 2005.
62. An adaptive locality-conscious process scheduler for embedded systems, by G.Chen, G.Chen, O.Ozturk, and M.Kandemir. In Proc. 11th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'05), San Francisco, California, March 2005.
63. Customized on-chip memories for embedded chip multiprocessors, by O.Ozturk, M.Kandemir, G.Chen, M.J.Irwin, and M.Karakoy. In Proc. the Asia and South Pacific Design Automation Conference (ASPDAC'05), Shanghai, China, January 2005.
64. Dynamic on-chip memory management for chip multiprocessors, by M.Kandemir, O.Ozturk, and M.Karakoy. In Proc. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES'04), Washington D.C., September 2004.

65. Data compression for improving SPM behavior, by O.Ozturk, M.Kandemir, I.Demirkiran, G.Chen, and M.J.Irwin. In Proc. the 41st Design Automation Conference (DAC'04), San Diego, CA, June 2004. (**Best Paper Candidate**)
66. Tuning data replication for improving behavior of MPSoC applications, by O.Ozturk, M.Kandemir, M.J.Irwin, and I.Kolcu. In Proc. the 2004 Great Lakes Symposium on VLSI (GLSVLSI'04), Boston, MA, April 26-28, 2004.